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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,435	04/25/2001	Brian William Hughes	10004546-1	7471

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 01/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/842,435	HUGHES ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 06 December 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☒ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☒ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *18-29*.

   Claim(s) withdrawn from consideration: *11-17*.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____

10. ☐ Other: _____

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133

Continuation of 2. NOTE: Claims 11-17 have been previously withdrawn and the amendment does not correctly indicate the withdrawal of claims 11-17.

Continuation of 5. does NOT place the application in condition for allowance because: Applicant's election with traverse of Group 11, claims 18-29 in the reply filed on 12/06/2004 is acknowledged. The traversal is on the ground(s) that "The invention of group 1 has already been searched by virtue of the Examiner's prior art rejection". This is not found persuasive because the language in independent claim 11 was modified to include language not previously considered in previous Office Actions and after the Examiner's last Office action. A search has not been completed for newly amended claims 11-17 filed 08/30/2004. The Examiner asserts that Group I is directed to testing and logging of test results whereas Group II is directed to remapping of faulty memory segments. They are two different inventions and require separate searches and actions.
The requirement is still deemed proper and is therefore made FINAL.

The Applicant contends, "As Eaton only discloses logically remapping defective memory locations, and not the physical remapping set forth in Claim 18, Eaton does not teach or suggest all the claim limitations found in Claims 18."
The Examiner disagrees and asserts that there is a one-to-one correspondence (i.e., a one-to-one mapping) between logical memory locations and physical memory locations. Any time a logical memory location is remapped so is the physical memory location corresponding to the logical memory location. The Examiner asserts that if a logical memory location is found faulty, then the physical memory location corresponding to the logical memory location is faulty; hence remapping of the logical memory location corresponding to the physical memory location allows the logical memory location corresponding to the physical memory location to be remapped to a replacement logical memory location corresponding to the replacement physical memory location. What good would it do to remap the logical memory location and not the physical memory location corresponding to the logical memory location since it is the physical memory location that is faulty? A one-to-one mapping between physical locations and logical locations ensures that the logical locations are substantially the physical locations as well. Hence Eaton teaches remapping defective physical memory locations.

The Applicant contends, "Eaton does not disclose a plurality of subsets of said memory segment wherein each subset comprises at least two linear arrays of elements."
The Examiner disagrees and asserts that rows and columns are linear arrays. Figure 3 in Eaton teaches multiple subsets of rows and columns of memory elements.

The Applicant contends, "Further, Eaton does not disclose that the records associated with his error correction code engine are made up of at least two linear arrays of elements". Nowhere does claim 22 recite any element concerning error correction code.

The Applicant contends, "The statements do not offer any motivation or reasons that the means of reading memory in Hams would have been of any benefit to the memory system of Eaton." Is the Applicant asserting that reading data out of memory has no benefit? The Examiner asserts that reading data out of memory has a definite benefit to the user of the data.

The Applicant contends, "The Examiner is arguing that one would be motivated to combine Eaton and Harns to provide a means for reading the memory of Hams, and that the modification would be obvious because it would have provided a means for reading the memory of Eaton." Even if the Applicant were correct, reading data out of memory still has a definite benefit to the user of the data.

The Applicant contends, "In addition, Eaton already has a means for reading the memory being tested (column 4, lines 48-57), there is no suggestion that a different means for reading the memory would be beneficial". The Examiner asserts that column 4, lines 48-57 explicitly recite a means for testing. Nowhere does Eaton discuss any specific means for reading data and nowhere is there any indication that the means for reading in Eaton are any different from the means in Harns since Eaton does not disclose a means for reading. What remains true in the Eaton patent is that a means for reading is a requirement for implementing the test system taught in Eaton. Providing a means for reading benefits the teachings in Eaton by providing a specific requirement for the test device in Eaton not taught in the Eaton patent. The test device in Eaton cannot be implemented without a specific means for reading data, hence it is highly desirable to modify the teaching in Eaton to include a specific means for reading data.